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10/675,706	01/09/2004	Young-Min Shin	8021-168 (SS-17883-US)	6305

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EXAMINER	
FLORES, LEON	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

C

Office Action Summary	Application No.	Applicant(s)	
	10/675,706	SHIN, YOUNG-MIN	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1-4 should be designated by a legend such as --***Prior Art***-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,577,692 B1 Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following analysis:

Current Application 10/675,706	US Patent 6,577,692 B1
Claim 1 the limitation: a master circuit, which includes a circuit to detect clock delay, receives a system reset signal, and generates output data, an output clock signal with which the output data is synchronized, and a reset control signal which responds to the system reset signal and a slave circuit in signal communication with the master circuit, where the slave circuit is reset in response to a reset control signal, receives the output clock signal and the output data, and sends to the master	Claims 1-3 *" a master circuit having a clock forward circuit" (claim 1)* *"control means for resetting the clock generator and the detecting means" (claim 3)* *"a slave circuit coupled to the master circuit for generating a second clock signal synchronized with the clock signal"* (claim 1) *"control means for resetting the clock generator and the detecting means"* (claim 3) *"wherein the input clock signal is a feedback clock signal of the output clock*

circuit an input clock signal as a feedback signal of the output clock signal and input data that is synchronized with the input clock signal wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to an initial parameter corresponding to the delay.	*signal" (claim 2)* *"detects a delay between the first and second signal, and sets initial data load/unload parameters of the master circuit based on the detected delay" (claim 1)* *"control means for resetting the clock generator and the detecting means when all detected delays are not equal" (claim 3)*
Claim 2 The digital system of claim 1, wherein the internal reset signal is a clock signal generated when detected delays are not identical to one another.	Claim 3 *"control means for resetting the clock generator and the detecting means when all detected delays are not equal".*
Re claim 3. A circuit to detect clock delay comprising: a delay detection circuit, which detects a delay between an output clock signal and	Claims 2-3 *"a delay detection circuit...."* (claim 2)

an input clock signal, generates an initial parameter corresponding to the delay if detected delays are identical to one another or continuously detects the delays until the detected delays are identical to one another if detected delays are not identical to one another, and generates a reset control signal in response to a system reset signal or an internal reset signal; and	*"control means for resetting the clock generator and the detecting means when all detected delays are not equal"* (claim 3)
a clock forwarding circuit in signal communication with the delay detection circuit, where the clock forwarding circuit loads and unloads input data in response to the initial parameter.	*"detects a delay between the first and second signal, and sets initial data load/unload parameters of the master circuit based on the detected delay"* (claim 1) *"a load/unload clock control ....."* (claim 2)
Re claim 4. The circuit of claim 3, wherein the delay detection circuit further comprises: a detection circuit, which is used to detect a delay between the output clock signal and	Claims 2-3. *"a delay detection circuit...."* (claim 2)

the input clock signal; a comparison circuit in signal communication with the detection circuit, which compares the detected delays and generates the initial parameter when the detected delays are identical to one another; and a control circuit in signal communication with the comparison circuit, where if detected delays are not identical to one another, resets the detection circuit, generates the reset control signal in response to the internal reset signal, and controls the comparison circuit to perform a comparison operation by N-bit free running until all the detected delays are identical to one another.	*"comparing means....."* (claim 3) *"control means....."* (claim 3)
Re claim 5. The circuit of claim 4, wherein the detection circuit comprises: a counting unit, which includes two D-type flip flops that are synchronized with the output clock signal and are reset by the input clock signal; and a detection unit in signal	Claim 4. *"a counting unit...."* (claim 4) *"a detecting unit...."* (claim 4)

communication with the counting unit, which receives output of the counting unit and detects the delay between the output clock signal and the input clock signal in response to the input clock signal.	
Re claim 6. The circuit of claim 4, wherein the comparison circuit further comprises: a latch unit, which includes a demultiplexer and N latches, respectively latches most significant bits and least significant bits of the delays outputted from the detection unit by N-bit free running; and a comparison unit in signal communication with the latch unit, which compares the most significant bits and least significant bits outputted from the latch unit, outputs one of the most significant bits and one of the least significant bits as the initial parameters, and outputs a first signal at a first level if all most significant bits and least significant bits are respectively	Claim 5. *"a latching unit...."* (claim 5) *"a comparing unit....."* (claim 5)

identical to one another, or outputs the first signal at a second level if all most significant bits and least significant bits are not respectively identical to one another.	
Re claim 7. The circuit of claim 6, wherein the control circuit comprises: an N-bit free running counter/decoder, which controls the demultiplexer to perform N-bit free running in response to the first signal and sends a predetermined clock signal to the latch unit; a system clock control unit in signal communication with the counter/decoder, which receives the clock signal in response to the first signal and outputs the clock signal as an internal reset signal; and a reset control unit in signal communication with the system clock control unit, which receives the system reset signal or the internal reset signal, sends the received system reset signal or internal reset signal to the N-bit free	Claim 6. *"an N-bit free running counter/decoder...."* (claim 6) *"a system clock control logic...."* (claim 6)

running counter/decoder, resets the detection unit, and outputs the system reset signal or the internal reset signal as the reset control signal.	
Re claim 8.	Claim 2.
The circuit of claim 7, wherein the clock forwarding circuit comprises: a clock generator, which is reset in response to output of the system clock control unit and	*"a clock generator..."* (claim 2)
generates the clock signal; an internal data bus in signal communication with the clock generator, which is used for data interface	*"an internal data bus..."* (claim 2)
with a predetermined master circuit; a data control unit in signal communication with the internal data bus, which is connected to the internal data bus and outputs data to a slave circuit in response to the clock	*"a data control logic...."* (claim 2)
signal; an output clock signal control unit in signal communication with the internal data bus, which outputs the output clock signal to the slave circuit in response to	*"an output clock control logic...."* (claim 2)

the clock signal; an input clock signal control unit in signal communication with the internal data bus, which receives and controls the clock signal and outputs the controlled clock signal; a load/unload clock control unit in signal communication with the internal data bus, which receives the controlled clock signal and generates load control signals and unload control signals in response to the initial parameter; and a load/unload multiplexer in signal communication with the internal data bus, which receives input data inputted from the slave circuit and unloads the input data to the internal data bus, through the data control unit, in response to the load control signals and the unload control signals.	*"an input clock control logic...."* (claim 2) *"a load/unload clock control logic...."* (claim 2) *"a load/unload multiplexer...."* (claim 2)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarvis (US Patent 5,918,040), and in view of applicant's prior art.

Re claim 1, the motivation for combining these two references has already been established in claim 12 below, therefore, the combination of Jarvis and applicant's prior art disclose that a digital system comprising: a master circuit, which includes a circuit to detect clock delay (In Jarvis, see Fig. 1: element 32, & see col. 2, lines 37-67.), receives a system reset signal, and generates output data, an output clock signal with which the output data is synchronized, and a reset control signal which responds to the system reset signal (In applicant's prior art, see paragraph 21.); and a slave circuit in signal communication with the master circuit, where the slave circuit is reset in response to a

reset control signal (In applicant's prior art, see paragraph 21.), receives the output clock signal and the output data, and sends to the master circuit an input clock signal as a feedback signal of the output clock signal and input data that is synchronized with the input clock signal (In applicant's prior art, see paragraph 8), wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to an initial parameter corresponding to the delay.(In applicant's prior art, see paragraphs 18 & 21.)

Claim 2 is a system claim corresponding to method claim 12. Hence, the steps in method claim 12 would have necessitated the elements in system claim 2 as claimed. Therefore, claim 2 has been analyzed and rejected w/r to claim 12 below.

Claim 3 is a system claim corresponding to method claim 12. Hence, the steps in method claim 12 would have necessitated the elements in system claim 3 as claimed. Therefore, claim 2 has been analyzed and rejected w/r to claim 12 below.

Re claim 4, the combination of Jarvis and applicant's prior art disclose that, wherein the delay detection circuit further comprises: a detection circuit, which is used to detect a delay between the output clock signal and the input clock signal; a comparison circuit in signal communication with the detection circuit, which compares the detected delays and generates the initial parameter when the detected delays are

identical to one another (These limitations have already been addressed in method claim 13. Hence, the steps in method claim 13 would have necessitated the elements as claimed. Therefore, these limitations have been analyzed and rejected w/r to claim 13 below); and a control circuit in signal communication with the comparison circuit, where if detected delays are not identical to one another, resets the detection circuit, generates the reset control signal in response to the internal reset signal, and controls the comparison circuit to perform a comparison operation by N-bit free running until all the detected delays are identical to one another. (The steps in method claim 14 would have necessitated the elements in system claim 4 as claimed. Therefore, these limitations have been analyzed and rejected w/r to claim 14 below.)

Claim 5 is a system claim corresponding to method claim 12. Hence, the steps in method claim 12 would have necessitated the elements in system claim 5 as claimed. Therefore, claim 5 has been analyzed and rejected w/r to claim 12 below.

Claim 6 is a system claim corresponding to method claim 13. Hence, the steps in method claim 13 would have necessitated the elements in system claim 6 as claimed. Therefore, claim 6 has been analyzed and rejected w/r to claim 13 below.

Claim 7 is a system claim corresponding to method claim 15. Hence, the steps in method claim 15 would have necessitated the elements in system claim 7 as claimed. Therefore, claim 7 has been analyzed and rejected w/r to claim 15 below.

Claim 8 is a system claim corresponding to method claim 16. Hence, the steps in method claim 16 would have necessitated the elements in system claim 8 as claimed. Therefore, claim 8 has been analyzed and rejected w/r to claim 16 below.

Claim 9 is a system claim corresponding to method claim 17. Hence, the steps in method claim 17 would have necessitated the elements in system claim 9 as claimed. Therefore, claim 9 has been analyzed and rejected w/r to claim 17 below.

Claim 10 is a system claim corresponding to method claim 18. Hence, the steps in method claim 18 would have necessitated the elements in system claim 10 as claimed. Therefore, claim 10 has been analyzed and rejected w/r to claim 18 below.

Claim 11 is a system claim corresponding to method claim 19. Hence, the steps in method claim 19 would have necessitated the elements in system claim 11 as claimed. Therefore, claim 11 has been analyzed and rejected w/r to claim 19 below.

Re claim 12, Jarvis discloses a method of detecting clock delay (In Jarvis, see abstract) comprising: (a) detecting a delay between an output clock signal and an input clock signal (see Fig. 2 & col. 4, lines 1-44 & col. 5, lines 1-64.) (b) continuously detecting the delay until the detected delays are identical to one another and generating a reset control signal in response to the system reset signal or the internal reset signal,

if the detected delays are not identical to one another (In Javis, see Fig. 2 & col. 4, lines 1-44 & col. 5, lines 1-64. If synchronization between the two devices is not achieved, then a new synchronization scheme must be initiated in order to establish synchronization. One skill in the art would know that if synchronization is not achieved between the two devices, one of the two devices, mainly the master circuit, will send a message to the other device, slave circuit, informing that they have not yet enter synchronization.). But the reference of Jarvis fails to specifically disclose generating an initial parameter corresponding to the delay if the detected delays are identical to one another, (c) loading and unloading input data in response to the initial parameter. However, applicant's prior art does. (See paragraphs 6 & 18.)

Applicant's prior art discloses that in a clock forwarding system, initial parameters are necessary for data loading and unloading. These initial parameters are computed once synchronization is achieved.

Taking the combined teachings of Jarvis and applicant's prior art as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated these steps into the system of Jarvis in the manner as claimed for the benefit of achieving synchronization between the master circuit and slave circuit.

Re claim 13, the combination of Jarvis and applicant's prior art further disclose that, wherein step (a) further comprises: (a1) detecting and outputting a delay between the output clock signal and the input clock signal (In applicant's prior art, see figures 1 & 2. One skill in the art would know that if a delay is computed at the receiving end, this

information will be sent to the transmitting end thus enabling the transmitter to adjust its parameter.); (a2) respectively latching most significant bits and least significant bits of the delays outputted in step (a1)(One skill in the art would know that in order to determine the delay between the clock out and clock in one must determine its edges.); and (a3) comparing the most significant bits and the least significant bits outputted in step (a2), outputting one of the most significant bits and one of the least significant bits as the initial parameters, and outputting a first signal (either 1 or 0 depending on the result of the comparison) at a first level if all most significant bits and least significant bits are respectively identical to one another, or outputting the first signal at a second level (either 1 or 0 depending on the result of the comparison) if all most significant bits and least significant bits are not respectively identical to one another. (In Jarvis, see figure 2. One skill in the art would know that in order to achieve synchronization a comparison of their edges must be computed.)

Re claim 14, the combination of Jarvis and applicant's prior art further disclose that, wherein step (b) is characterized by generating the reset control signal for resuming step (a) in response to the first signal if one of the detected delays is not identical to other detected delays and resuming step (a) by N-bit free running until the detected delays are identical to one another. (In Jarvis, see Fig. 2.)

Re claim 15, the combination of Jarvis and applicant's prior art further disclose that, wherein step (b) further comprises: (b1) generating an internal reset signal in

response to the first signal and a predetermined clock signal (In Jarvis, see Fig. 2. When Mo is not equal to So a new Mo or So must be computed in order to achieve synchronism. Furthermore, in applicant's prior art, see paragraph 21.); (b2) receiving the system reset signal or the internal reset signal, and generating the reset control signal (In Jarvis, see Fig. 2, Once the determination that Mo is not equal to So, a feedback loop is generated and a new value must be computed in order to synchronize the master circuit and the slave circuit. Furthermore, in applicant's prior art, see paragraph 21.); and (b3) performing N-bit free running in response to the first signal and generating an N-bit free running signal (In Jarvis, see Fig. 2, Once the determination that Mo is not equal to So, a feedback loop is generated and a new value must be computed in order to synchronize the master circuit and the slave circuit.)

Re claim 16, the combination of Jarvis and applicant's prior art further disclose that, wherein step (c) further comprises: (c1) generating the clock signal; (c2) outputting the output clock signal to a slave circuit in response to the clock signal; (c3) receiving and controlling the clock signal, and outputting the controlled clock signal; (c4) receiving the controlled clock signal, and generating load control signals and unload control signals in response to the initial parameter; and (c5) receiving input data inputted from the slave circuit, and unloading the input data in response to the load control signals and the unload control signals. (In applicant's prior art, see paragraphs 6-18. One skilled in the art would know that this is how a system that utilizes clock forwarding as a

mechanism to achieve synchronization would operate.)

Re claim 17, the combination of Jarvis and applicant's prior art further disclose that, wherein the output clock signal is outputted from a predetermined master circuit, the input clock signal is outputted from a predetermined slave circuit, and the input clock signal is a feedback clock of the output clock signal. (In applicant's prior art, see paragraphs 6-10.)

Re claim 18, the combination of Jarvis and applicant's prior art further disclose that, wherein the internal reset signal is generated when the detected delays are not identical to one another. (In Jarvis, see Fig. 2, where an internal reset signal is generated when Mo is not equal to So. Furthermore, in applicant's prior art, see paragraph 21.)

Re claim 19, the combination of Jarvis and applicant's prior art further disclose that, wherein the reset control signal is generated when the system reset signal or the internal reset signal is activated. (In applicant's prior art, see paragraph 21. Furthermore, see claim 18.)

Claim 20 is a system claim corresponding to method claim 12. Hence, the steps in method claim 12 would have necessitated the elements in system claim 20 as

claimed. Therefore, claim 20 has been analyzed and rejected w/r to claim 12 below. Furthermore, the limitations in this claim has already been addressed in system claim 3.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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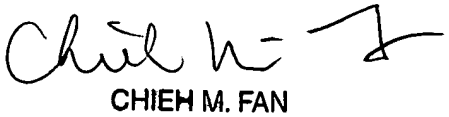
December 15, 2006



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